WHAT IS CLAIMED IS:

1. A memory cell, comprising:

a pillar of semiconductor material that extends outwardly from a working surface of a substrate to form source/drain and body regions, the pillar having a number of sides;

more than two floating gates, each gate associated with a side of the pillar; and

a number of control gates, each control gate associated with at least one floating gate so as to allow selective storage and retrieval of data on the floating gates.

2. The memory cell of claim 1, wherein the substrate is a bulk semiconductor.

3. The memory cell of claim 1, wherein the working surface of the substrate includes an insulating layer formed on top of an underlying semiconductor.

4. The memory cell of claim 1, wherein the control gate is capable of storing more than two charge states on its associated floating gate.

5. A memory device, comprising:

an array of memory cells, each cell including a number of transistors formed around a common pillar of semiconductor material that forms source/drain and body regions for the transistors and a number of floating gates disposed adjacent to the sides of the pillar;

a plurality of first gate lines that are substantially parallel in a first direction, each first gate line allowing selective storage and retrieval of data on ones of the floating gates;

a plurality of second gate lines that are substantially parallel in a second direction that is substantially orthogonal to the first direction, each second gate line allowing selective storage and retrieval of data on ones of the floating gates;

at least one first source/drain interconnection line, interconnecting ones of the first source/drain regions of ones of the memory cells; and

a plurality of data lines, each data line interconnecting ones of the second source/drain regions of ones of the memory cells.

6. The memory device of claim 5, wherein the pillar extends outwardly from a bulk semiconductor substrate.

7. The memory device of claim 5, wherein the pillar extends outwardly from an insulating layer portion formed on top of an underlying semiconductor substrate.

8. A memory device, comprising:

an array of memory cells, each cell including a number of transistors formed around a common pillar of semiconductor material that forms source/drain and body regions for the transistors and more than two gates disposed adjacent to the sides of the pillar;

a plurality of first gate lines interconnecting ones of the gates in ones of the memory cells;

a plurality of second gate lines interconnecting ones of the gates in ones of the memory cells;

at least one first source/drain interconnection line interconnecting ones of the first source/drain regions of ones of the memory cells; and

a plurality of data lines, each data line interconnecting ones of the second source/drain regions of ones of the memory cells.

9. The memory device of claim 8, wherein the pillar extends outwardly from a bulk semiconductor substrate.

10. The memory device of claim 8, wherein the pillar extends outwardly from an insulating layer portion formed on top of an underlying semiconductor substrate.

11. The memory device of claim 8, wherein the first gate lines are substantially parallel in a first direction.

12. The memory device of claim 8, wherein the second gate lines are substantially parallel in a second direction that is substantially orthogonal to the first direction.

13. The memory device of claim 8, wherein the at least one first source/drain interconnection line is formed at least partially within the substrate.

14. A memory cell that is fabricated upon a substrate, the memory cell comprising:

a first conductivity type semiconductor pillar, having top and side surfaces and formed upon the substrate;

a first source/drain region, of a second conductivity type, formed proximal to an interface between the pillar and the substrate;

a second source/drain region, of a second conductivity type, formed in a portion of the pillar that is distal to the substrate and separate from the first source/drain region;

a gate dielectric formed on at least a portion of the side surface of the pillar;

more than two floating gates, each of which is substantially adjacent to a portion of the side surface of the pillar and separated therefrom by the gate dielectric;

a plurality of control gates, each of which is substantially adjacent to one of the floating gates and insulated therefrom; and

an intergate dielectric, interposed between each of the substantially adjacent floating and control gates.

15. The memory cell of claim 14, wherein the substrate includes a bulk semiconductor from which the pillar outwardly extends.

16. The memory cell of claim 14, wherein the substrate includes an insulating layer from which the pillar outwardly extends.

17. A nonvolatile memory array that is fabricated upon a substrate, the memory array comprising:

a plurality of memory cells, each memory cell including:

a first conductivity type semiconductor pillar, having top and side surfaces and formed upon the substrate;

a first source/drain region, of a second conductivity type, formed proximal to an interface between the pillar and the substrate;

a second source/drain region, of a second conductivity type, formed in a portion of the pillar that is distal to the substrate and separate from the first source/drain region;

a gate dielectric, formed on at least a portion of the side surface of the pillar;

more than two floating gates, substantially adjacent to a portion of the side surface of the pillar and separated therefrom by the gate dielectric;

at least one control gate, substantially adjacent to the floating gate and insulated therefrom; and

an intergate dielectric; interposed between the floating gate and the control gate;

a plurality of first gate lines interconnecting ones of the control gates in ones of the memory cells;

a plurality of second gate lines interconnecting ones of the control gates in ones of the memory cells;

at least one first source/drain interconnection line interconnecting ones of the first source/drain regions of ones of the memory cells; and

a plurality of data lines, each data line interconnecting ones of the second source/drain regions of ones of the memory cells.

18. The memory array of claim 17, wherein the substrate includes a bulk semiconductor from which the pillar outwardly extends.

19. The memory array of claim 17, wherein the substrate includes an insulating layer from which the pillar outwardly extends.

20. The memory array of claim 17, wherein the first gate lines are substantially parallel in a first direction.

21. The memory array of claim 17, wherein the second gate lines are substantially parallel in a second direction that is substantially orthogonal to the first direction.

22. The memory array of claim 17, wherein the at least one first source/drain interconnection line is formed at least partially within the substrate.

23. The memory array of claim 17, wherein the first gate lines are formed at least partially within the substrate.

24. The memory array of claim 17, wherein the second gate lines are formed substantially above the substrate.

25. A method of forming a memory array, the method comprising the steps of:

forming a plurality of first conductivity type semiconductor pillars upon a substrate, each pillar having top and side surfaces;

forming a plurality of first source/drain regions, of a second conductivity type, each of the first source/drain regions formed proximally to an interface between the pillar and the substrate;

forming a plurality of second source/drain regions, of a second conductivity type, each of the second source/drain regions formed within one of the pillars and distal to the substrate and separate from the first/source drain region;

forming a gate dielectric on at least a portion of the side surface of the pillars;

forming more than two floating gates per pillar, each of the floating gates formed substantially adjacent to a portion of the side surface of one of the pillars and separated therefrom by the gate dielectric;

forming a plurality of control gates, each of the control gates formed substantially adjacent to at least one of the floating gates and insulated therefrom;

forming a intergate dielectric, interposed between ones of the floating gates and ones of the control gates;

forming a plurality of first gate lines, each first gate line interconnecting ones of the control gates;

forming a plurality of second gate lines, each second gate line interconnecting ones of the control gates;

forming at least one first source/drain interconnection line interconnecting ones of the first source/drain regions; and

forming a plurality of data lines, each data line interconnecting ones of the second/source drain regions.

26. The method of claim 25, further comprising the step of forming an insulating layer between the semiconductor pillars and a semiconductor portion of the substrate.

27. The method of claim 25, wherein the first gate lines are formed substantially parallel in a first direction.

28. The method of claim 25, wherein the second gate lines are formed substantially parallel in a second direction that is substantially orthogonal to the first direction

29. The method of claim 25, wherein the at least one first source/drain interconnection line is formed at least partially within the substrate.

30. The method of claim 25, wherein the step of forming the plurality of first gate lines is carried out at least partially within the substrate.

31. The method of claim 25, wherein the step of forming the plurality of second gate lines is carried out substantially above the substrate.

32. The method of claim 25, wherein the step of forming the plurality of pillars further comprises the steps of:

growing an epitaxial layer on the substrate;

etching the epitaxial layer and a portion of the underlying substrate to form a plurality of first troughs therein for carrying the first gate lines; and

etching the epitaxial layer to form therein a plurality of second troughs, substantially orthogonal to the plurality of first troughs, the second troughs for carrying the second gate lines.

33. The method of claim 32, wherein the step of forming more than two floating gates per pillar comprises the steps of:

depositing polysilicon in the first troughs; and

etching the deposited polysilicon in a median portion of the first troughs to form ones of the floating gates on either side of the first troughs, each floating gate adjacent to one of the pillars but separated therefrom by the gate dielectric.

34. The method of claim 33, wherein the steps of forming the plurality of first gate lines comprises the steps of:

etching into the substrate in a median portion of the first troughs; and

depositing conductive polysilicon in and above the substrate in the etched median portion of the second troughs to form the first gate lines in the substrate and ones of the control gates above the substrate.

35. The method of claim 33, wherein the step of forming the plurality of floating gates further comprises the steps of:

depositing conductive polysilicon in the second troughs; and

etching the deposited polysilicon in a median portion of the second troughs to form ones of the floating gates on either side of the second troughs.

36. The method of claim 25, wherein the step of forming the plurality of second gate lines comprises the step of depositing conductive polysilicon in the etched median portion of the second troughs.

37. The method of claim 25, wherein the step of forming the plurality of second source/drain regions comprises the step of ion-implanting a dopant of the second conductivity type.

38. The method of claim 25, wherein the step of forming the gate dielectric comprises the step of growing on the side surface of each pillar a layer of silicon dioxide of thickness approximately between 5 nanometers and 10 nanometers.

39. The method of claim 25, wherein the step of forming the plurality of data lines comprises the steps of:

depositing an insulator over the pillars, the floating and control gates, and first and second gate lines;

forming contact holes in the insulator to contact the second/source drain regions of each pillar;

depositing a conductive layer on the insulator and in the contact holes; and

etching the conductive layer to form the resulting data lines.

40. A method of forming a memory array on a substrate, the method comprising the steps of:

forming a first source/drain layer at a surface of the substrate;

forming a semiconductor epitaxial layer on the first source/drain layer;

forming a second source/drain layer at a surface of the epitaxial layer;

etching, in a first direction, a plurality of substantially parallel first troughs in the epitaxial layer;

forming a first gate dielectric layer substantially adjacent to sidewall regions of the first troughs;

forming a first conductive layer in the first troughs;

removing a portion of the first conductive layer in the first troughs such that floating gate regions are formed along the sidewall regions therein and separated from the sidewall regions by the first gate dielectric layer;

etching a portion of the substrate underlying a portion of the first troughs between the floating gate regions;

forming a first intergate dielectric layer on exposed portions of the floating gate regions in the first troughs;

forming first gate lines in the underlying etched portion of the substrate between opposing floating gate regions in the first troughs; and

forming control gate regions in the first troughs between opposing floating gate regions and separated therefrom by the first intergate dielectric layer.

41. The method of claim 40, further comprising the steps of:

etching, in a second direction that is substantially orthogonal to the first direction, a plurality of substantially parallel second troughs in the epitaxial layer;

forming a second gate dielectric layer substantially adjacent to sidewall regions of the second troughs;

forming a second conductive layer in the second troughs;

removing a portion of the second conductive layer in the second troughs such that floating gate regions are formed along the sidewall regions therein and separated from the sidewall regions by the second gate dielectric layer;

forming a second intergate dielectric layer on exposed portions of the floating gate regions in the second troughs; and

forming control gate regions and second gate lines between opposing floating gate regions in the second troughs and separated from the floating gate regions in the second troughs by the second intergate dielectric layer.

42. The method of claim 40, wherein the substrate is a bulk semiconductor.

43. The method of claim 40, wherein the substrate includes a semiconductor on insulator portion.

44. The method of claim 40, further comprising the step of forming an insulating layer undercutting semiconductor regions between the first troughs.